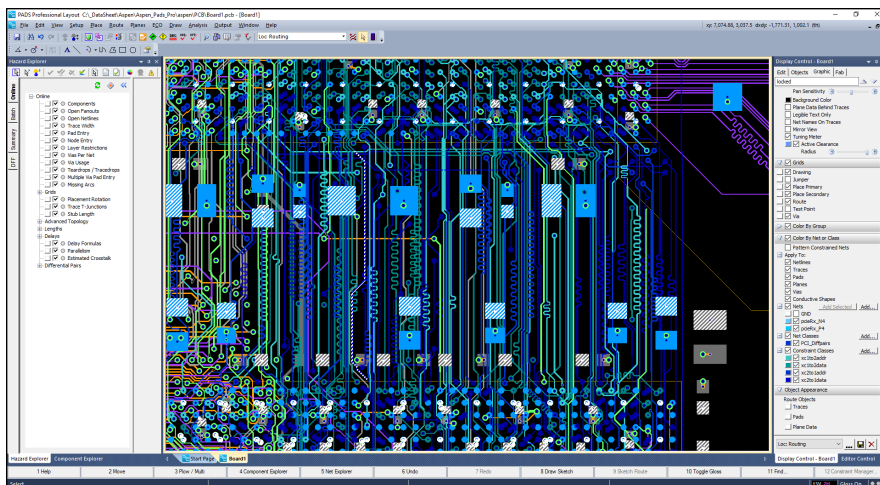




## Multi-Trace High-Speed Design (HSD) Tuning Option For PADS Professional



*Designing with high-speed nets? Reduce design time with multi-trace high-speed tuning for quick definition, tuning, and review of complex nets.*

### MAJOR BENEFITS:

- Review and resolve hazards for topology and high-speed design rules
- Quickly define, tune, and review complex nets
- Conduct 'what-if' experiments with push-button sketch route and auto-tune capabilities
- Quickly match lengths of high-speed routes
- Consider electrical delay requirements when working with advanced topologies such as DDR

### OVERVIEW

High-speed memory interfaces and other sensitive connections multiply design complexity. Designers need more advanced tools to meet tighter and tighter constraints. The PADS Professional Multi-Trace HSD Tuning option offers high-speed design features and automation to reduce design time by quickly defining, tuning, and reviewing complex nets. Multiple methods for tuning traces in your design are provided to quickly match lengths of high-speed routes.

### High-Speed Route Tuning

Manual tune gives the designer more control to precisely add length to meet the most complex constraint definitions. Open up dense areas of a board to add length to traces where needed, while preserving existing tune structures.

Auto-tune uses the constraint's definitions providing a one-button tune that meets electrical delay requirements, enabling you to minimize re-work and ensure your designs will meet the most stringent timing definitions (Figure 1).

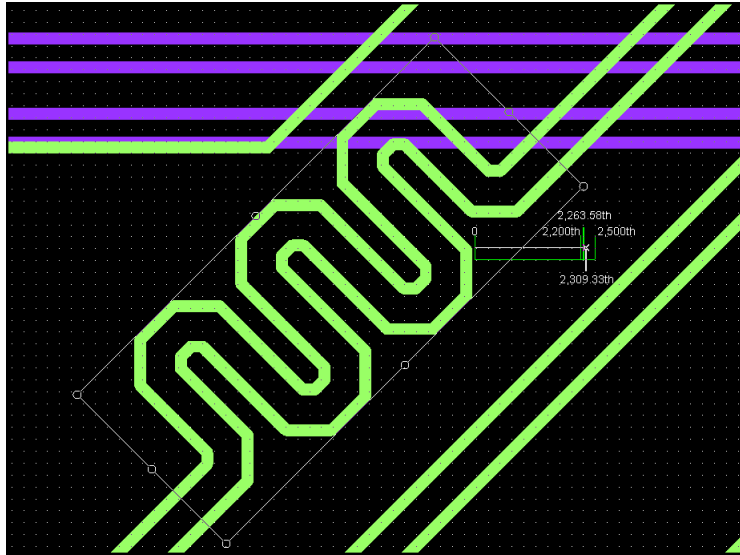


Figure 1: With multi-trace tuning, you can preserve existing structures while adding trace length as needed to meet timing requirements.

### Leverage Auto-Tune with Sketch Route

After routing bundles of nets with sketch route, use auto-tune to quickly tune nets with a push of a button. With the speed of sketch route and auto-tune you can leverage the two-step process as a 'what-if' procedure. Quickly lay down traces, tune, and decide whether the traces are optimal. If there is little room, simply undo the routing and change the floor plan or route path.

### High-Speed Constraints

Define length and topology constraints in the constraint manager to complete timing-sensitive designs faster and to ensure electrical requirements are always met. DDR and other advanced topology networks can be quickly set up using match groups or formulas to take complex, inter-dependent delay requirements into consideration. Also, include package and via lengths into your length calculations. Gain control over the rules needed for high-speed designs. With PADS Professional, you can establish rules between any of the grouping structure (classes, layers, and nets) and set matched length, maximum/minimum length, and differential pairs.

### Online DRC Rules

Minimize board re-spins by reviewing your design violations in an organized spreadsheet. Simplify the review process between multiple designers by accepting or adding comments to violations. If you decide to resolve an issue, simply click on a violation to cross probe to the affected area. The hazards will interactively update as you route, tune, and move traces.

PADS Professional HSD Tuning adds high-speed DRCs for advanced topologies and offers more differential pairs checks. View delay formula violations, length/delay tolerance, parallelism, differential pairs out of convergence, and other high-speed checks.

### Parallelism Rules

The constraint manager provides a simple dialog box for parallelism rule creation and assignment. Parallelism rules apply on the same or adjacent layers and can be assigned at the net or class level for maximum control and flexibility. Use Hazard Explorer to view parallelism violations, then automatically resolve the violations (Figure 2) by adding spacer objects to separate the traces.



Figure 2: Use Hazard Explorer to view and resolve Parallelism rules (definition not shown).

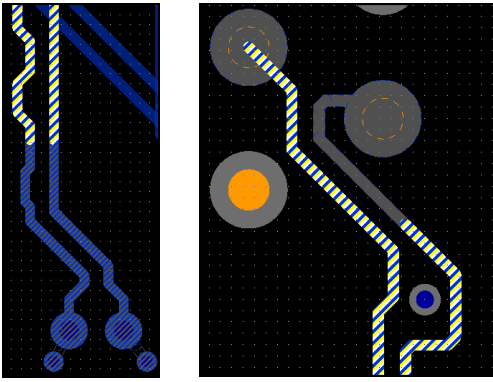


Figure 3: Use Hazard Explorer to find oversized saw-tooth patterns that violate separation distance (left) and to identify objects that cause split differential pairs (right).

### Differential Pair Rules

Separation distance can be used to identify an oversized saw tooth pattern, or other obstructions that cause the differential pair to split. Clicking on the violation in Hazard Explorer automatically highlights the offending trace structure or trace (Figure 3).

Differential Pair Length Tolerance identifies length differences between the two nets, usually due to non-symmetric escape patterns (Figure 4). Quickly cross probe to the start of the offending structure and fix the escape pattern symmetry.

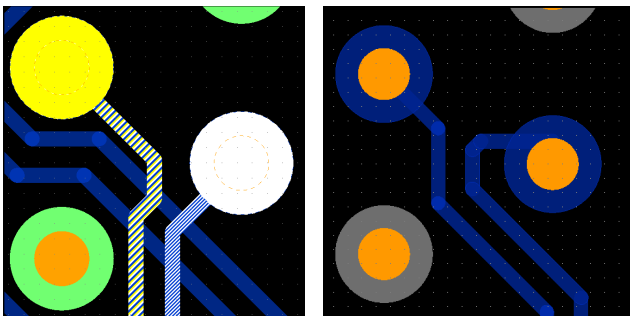


Figure 4: Find and fix non-symmetric escape patterns by identifying trace-length differences and crossprobing to the beginning of the structure.

### Target Length Dialog

View constraint-dependent nets by selecting one net. Sort and view the longest net of the bunch to plan your attack. Cross probe and select nets of interest for manual tuning or tune the bunch using auto-tune (Figure 5).

Target	Range	Solution	Current	Deviation	Manhattan...	Meander	Cluster Source	Net Name
	1,439.67 - 1,599.67	1,599.67	1,635.4	45.73	1,501.95	21%	user-defined	DDR2_LOWER_DAT
	1,439.67 - 1,489.67	1,489.67	1,635.75	137.08	1,471.84	114.4%	user-defined	DDR2_DATA23
	1,439.67 - 1,489.67	1,489.67	1,624.95	135.18	1,390.14	16.9%	user-defined	DDR2_DATA31
	1,439.67 - 1,489.67	1,489.67	1,623.74	134.07	1,549.53	4.8%	user-defined	DDR2_DATA18
	1,439.67 - 1,489.67	1,489.67	1,618.44	128.77	1,255.49	28.9%	user-defined	DDR2_DATA30

Figure 5: The Target Length dialog box helps in route planning and manual and automatic tuning.

### Virtual Pin Manipulation

When defining topologies, use virtual pins as balance or branch points between a driver and multiple loads. Virtual Pins are automatically placed in layout and can be manually moved and associated with a via. Once associated, the virtual pin and via move in sync (Figure 6).

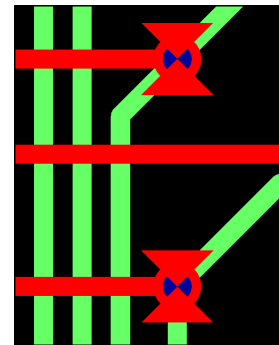


Figure 6: Use virtual pins as balance or branch points between a driver and multiple loads. They'll move in sync with associated vias.



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